Remarks/Arguments

The Office Action dated September 16, 2003, has been carefully reviewed and the foregoing amendments made in response thereto. Examiner's acknowledgement of applicant's claim for foreign priority under 35 U.S.C. § 119(a)-(d) is noted with appreciation. Reconsideration of the grounds of objections and rejections is respectfully requested in view of the above amendments and the remarks herein.

Claims 1-12 have been canceled.

Claims 13-48 are pending in the application.

Claims 27 and 28 stand objected to under 37 CFR 1.75(c) for failing to further limit the subject matter of a previous claim. Claims 23, 31, 37, and 42 stand objected to for informalities. Claims 13-48 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Pat. No. 5,983,326 to Hagersten, et al. (hereafter referred to as "Hagersten").

The Objections to Claims 23, 27, 28, 31, 37, and 42

Claims 27 and 28 have been amended to overcome the objection under 37 CFR 1.75(c). Claims 23, 31, 37, and 42 have been amended to overcome the informality objection.

Rejection of Claims 13 and 31 under 35 U.S.C. 102(e)

According to MPEP § 2131, "To anticipate a claim, the reference must teach every element of the claim." The Hagersten reference does not teach every element of the rejected claims of the present invention. The Examiner's rejections under 35 U.S.C. § 102(e) are generally premised on the conclusion that the system interface (24) of Hagersten anticipates the connection agents (NCSi) and the external

connection nodes (NCEj) of the present invention. Admittedly, Hagersten's system interface (24) does perform the function of interconnecting the processors on two levels; however, the system interface (24) achieves this interconnection through an implementation and architecture that is fundamentally different than the claimed invention. Hagersten describes, at column 16, lines 54-66, "Transactions from SMP in queue 94 and SMP PIQ 96 are processed by a request agent 100 within system interface 24." Further, Hagersten states, at column line, "[a]lso included in system interface 24 is a home agent 102 and a slave agent 104. Home agent 102 processes coherency requests received from input header queue 84." The system interface (24) comprises request agents (100), home agent (102), and slave agent (104). Each of these agents differ from each other in architecture and function. Figures 5 of Hagersten shows the different external interfaces between the request agent, home agent and slave agent. The Examiner draws a comparison between home agent (102) and the connection agents (NCSi) and the external connection nodes (NCEj). In the claimed invention, the applicants teach connection agents (NCSi) and the external connection nodes (NCEj) that have the same basic structure, the same external interface (XI), and are adapted to implement the same coherency control protocol for the cache memories of the processors. See claim 13, last four lines. Hagersten does not teach this construction. Nor does Hagersten or the other prior art suggest this construction.

Turning to the specific rejections, as noted above, Claim 13 recites, inter alia, the connection agents (NCSi) and the external connection nodes (NCEj) respectively having the same basic structure, having the same external interface (XI), and adapted to implement the same coherency control protocol for the cache memories of the processors. Hagersten does not teach this feature of the invention. Hagersten states at

column 9, lines 23-25, "System interface 24 provides internode coherency, while snooping upon SMP bus 20 provides intranode coherency." In contrast, Claim 13 of the present invention teaches utilizing nodes having the same architecture, external interface, and implementing the same coherency control protocol for both inter and intra node coherency.

Claim 31 recites, inter alia, an expandable multinode multiprocessor machine where the connection agents (NCSi) and the external connection nodes (NCEj) respectively, like the construction of claim 13, have the same architecture, the same external interface (XI), and are adapted to implement the same coherency control protocol for the cache memories of the processors. Hagersten does not teach this feature of the claimed invention.

Accordingly, withdrawal of the rejection of claims 13 and 31 under 35 U.S.C. § 102(e) is respectfully requested.

Rejection of Claims 14-32, 15-16, and 33-34

At the outset, claims 14 and 32, 15-16 and 32-34, depend either directly or through intermediary claims on claims 13 and 31. Thus the claims are believed to patently distinguish Hagersten for the same reasons previously set forth herein. Additionally the claims are believed to be patentable in their own right based on the limitations set forth therein.

Claims 14 and 32 recite, inter alia, two identical connection agents (NCSi) connected head-to-tail, one of the two agents (NCS'j) receiving and filtering transactions sent by the node (Nj) to which it is connected, and the other agent (NCS"j) receiving and filtering the transactions sent by the other nodes (Nj) to which it is connected. Hagersten does not teach a system interface (24) comprised of two

identical agents connected in a head-to-tail arrangement. In Hagersten, Figure 3 depicts the system interface 24, which does not teach identical agents connected in a head to tail arrangement. In fact, Hagersten's home agent 102, slave agent 102, and request agent 100 are shown in Figure 3 to be not identical and not connected in a head to tail arrangement.

Claims 15-16 and 33-34 recite, inter alia, that each connection agent (NCSi) comprises an associative memory (DDi) with a fixed size determined as a function of the number of processors in the multiprocessor module (QPi) to which the connection agent (NCSi) is connected, the state of the memories (DDi) being indicative of the presence of the last modified data blocks in the cache memories of the multiprocessor module (QPi). The associative memory (DDi) performs the function of storing the state of the cache memories within the multiprocessor module. Hagersten does not teach, in system interface (24), an associative memory corresponding to the number of processors for the purpose of storing the indication of the last modified data blocks in the cache memories of the multiprocessor module.

Accordingly, withdrawal of the rejection of claims 14 and 32, 15-16 and 32-34 is respectfully requested.

Rejection of Claims 17 and 35, 18-22, and 36

At the outset, claims 17 and 35, 18-22, and 36, depend either directly or through intermediary claims on claims 13 and 31. Thus the claims are believed to patently distinguish Hagersten for the same reasons previously set forth herein. Additionally the claims are believed to be patentable in their own right based on the limitations set forth therein.

Applicant has carefully examined the text of Hagersten column 13, lines 27-59 and there is nothing in the text to suggest an associative memory residing within the connection agents themselves. In Hagersten the coherency state is stored within the memory 22, which is the memory of computer system 10, memory 22 is not located within the connection agents.

Claims 17 and 35 recite, inter alia, first and second head-to-tail connection agents (NCS'j and NCS"j) that only accept transactions for blocks modified in their respective associative memories (DD'j and DD"j); modified data blocks in the first connection agent (NCS'j) being exported to the requesting multiprocessor module or modules and, conversely, modified data blocks in the second connection agent (NCS"j) being imported from the module or modules holding the blocks. Hagersten teaches, at column 16, lines 6-8, "System interface 24 also includes input and output queues for storing transactions to be performed upon SMP bus 20 or network 14." The claimed invention patently distinguishes from Hagersten by claiming that the two head-to-tail connection agents (NCS'j and NCS"j) only accept transactions for blocks modified in their respective memories. This arrangement of connection agents is architecturally and functionally distinct from Hagersten's system interface (24).

Accordingly, withdrawal of the rejection of claims 17 and 35, 18-22, and 36 is respectfully requested.

Rejection of Claims 23-30 and 37-48

As the Examiner noted, Claims 23-30 and 37-48 encompass the same scope of invention as claims 13-18, but are drafted as method claims. Accordingly, arguments above relating to claims 13-18 are also applicable to the rejection of claims 23-30 and 37-48.

Accordingly, withdrawal of the rejection of claims 23-30 and 37-48 is respectfully requested.

Summary

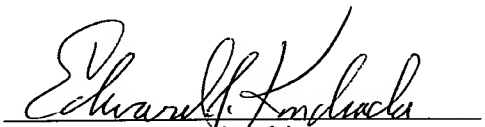
In view of the foregoing, Applicants believe claims are in condition for allowance and respectfully request withdrawal of the objections and rejections. Passage of the case to issue at an early date is earnestly solicited inasmuch as the application is believed to be in condition for allowance. Should the Examiner believe that one or more issues remain unresolved, in order to more expeditiously resolve any such remaining issues, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

Authorization is hereby given to charge any additional fee that is deemed to be due or necessary as a result of the filing of this Amendment, to Deposit Account No. 501165. A duplicate copy of this paper is enclosed for deposit account charging purposes.

Respectfully submitted,

Miles & Stockbridge P.C.

Date: December 8, 2003

By: 
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